Analysis and Synthesis of Synchronous Sequential Circuits

The Synchronous Sequential Circuit Model

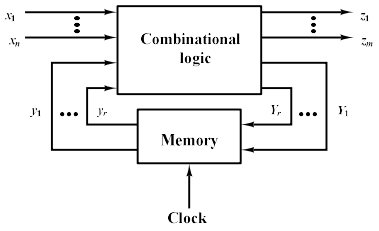


Figure 8.1

Mearly-Moore Machine Model

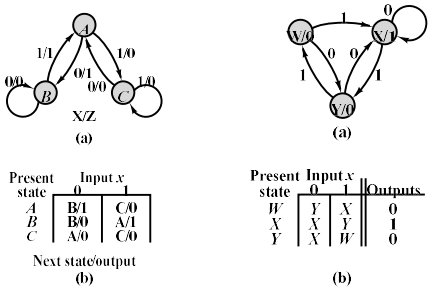


Figure 8.4

Mealy Machine Model

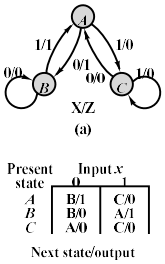


Figure 8.2

Mealy Machine Timing Diagram -- Example 8.1

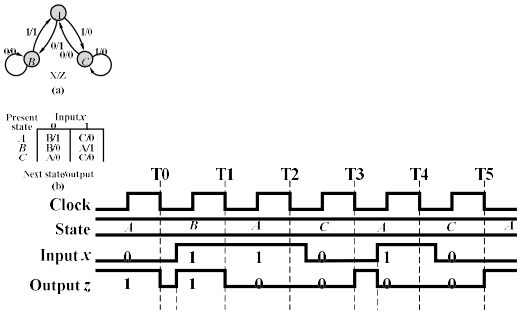


Figure 8.3

Moore Machine Timing Diagram -- Example 8.2

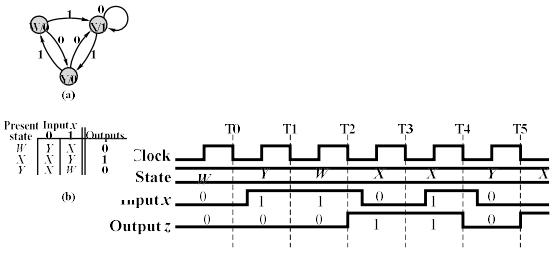


Figure 8.5

Analysis of Sequential Circuit State Diagrams -- Example 8.3

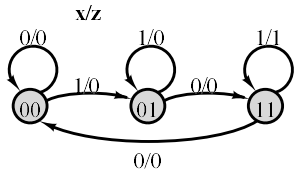


Figure 8.6

Timing Diagram for Example 8.3

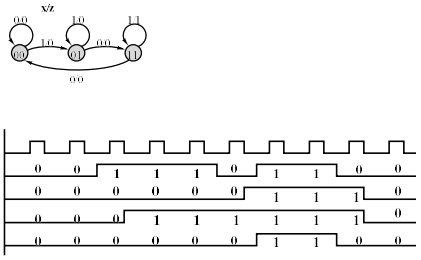


Figure 8.7

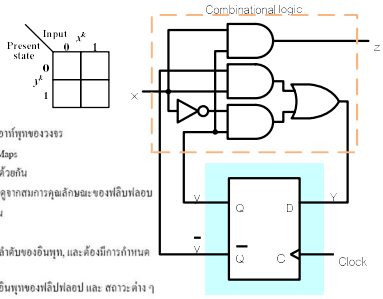
ขั้นตอนการวิเคราะห์วงจรซิงโครนัสซีเควนเชียล

1. หาสมการอินพุทของฟลิปฟลอปและสมการเอาท์พุทของวงจร
2. นำสมการที่ได้จากข้อ 1 แทนลงในตาราง K-Maps
3. รวมตารางอินพุทของฟลิปฟลอปแต่ละตัวเข้าด้วยกัน
4. สร้างตารางสภาวะถัดไป (next state) ด้วยการดูจากสมการคุณลักษณะของฟลิปฟลอบ
5. รวมตารางสภาวะถัดไปกับเอาท์พุทเข้าด้วยกัน
6. สร้างสเตทไดอะแกรม
7. เขียนไทม์มิ่งไดอะแกรมที่มีสัญญาณนาฬิกา, ลำดับของอินพุท, และต้องมีการกำหนดสภาวะเริ่มต้นด้วย
8. จากไทม์มิ่งไดอะแกรมทำการหารูปคลื่นด้านอินพุทของฟลิปฟลอป และ สถาวะต่าง ๆ ทั้งของฟลิปฟลอบและวงจร
9. ทำการหารูปคลื่นเอาท์พุทของวงจร

Analysis of Sequential Circuit Logic Diagrams

$D = Y = x\bar{y} + \bar{x}y$

$Z = xy$



1. หาสมการอินพุทของฟลิปฟลอปและสมการเอาท์พุทของวงจร
2. นำสมการที่ได้จากข้อ 1 แทนลงในตาราง K-Maps
3. รวมตารางอินพุทของฟลิปฟลอปแต่ละตัวเข้าด้วยกัน
4. สร้างตารางสภาวะถัดไป (next state) ด้วยการดูจากสมการคุณลักษณะของฟลิปฟลอบ
5. รวมตารางสภาวะถัดไปกับเอาท์พุทเข้าด้วยกัน
6. สร้างสเตทไดอะแกรม
7. เขียนไทม์มิ่งไดอะแกรมที่มีสัญญาณนาฬิกา, ลำดับของอินพุท, และต้องมีการกำหนดสภาวะเริ่มต้นด้วย
8. จากไทม์มิ่งไดอะแกรมทำการหารูปคลื่นด้านอินพุทของฟลิปฟลอป และ สถาวะต่าง ๆ ทั้งของฟลิปฟลอบและวงจร
9. ทำการหารูปคลื่นเอาท์พุทของวงจร

Figure 8.8

State Table and State Diagram for Figure 8.8 (a)

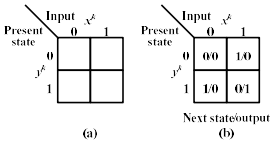


Figure 8.10

K-Maps for Circuit of Figure 8.8 (a)

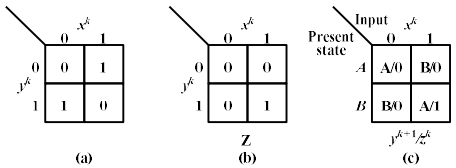


Figure 8.11

Timing Diagram for Figure 8.8 (a)

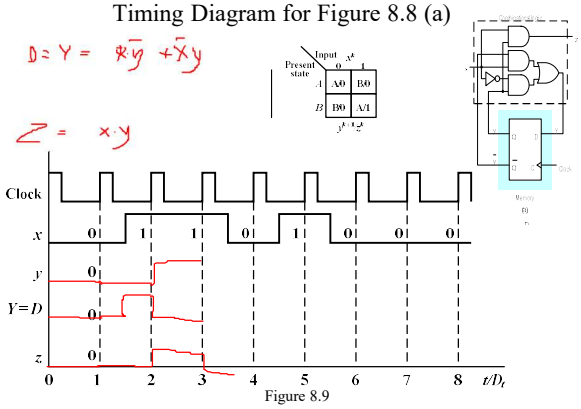


Figure 8.9

Timing Diagram for Figure 8.8 (a)

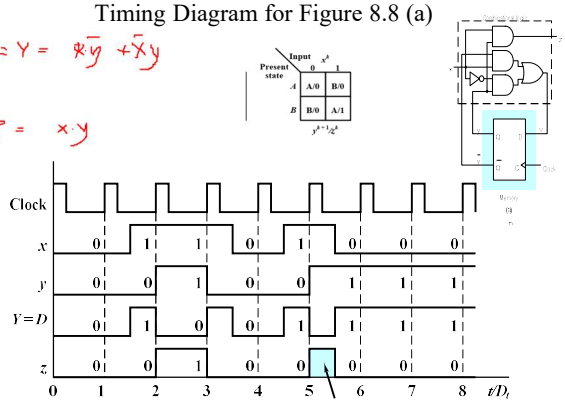


Figure 8.9

Synchronous Sequential Circuit with T Flip-Flop -- Example 8.4

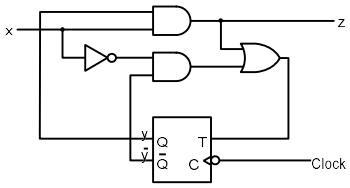


Figure 8.12

K-Maps for Example 8.4

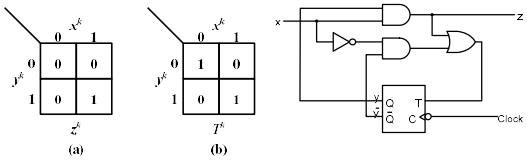


TABLE 6.3 SUMMARY OF LATCH AND FLIP-FLOP CHARACTERISTICS

Device	Characteristic Equation
SR latch	$Q^* = S + \bar{R}Q$
Gated SR latch	$Q^* = SC + \bar{Q}R + \bar{C}Q$
D latch	$Q^* = DC + \bar{C}Q$
SR flip-flop	$Q^* = S + \bar{R}Q$
D flip-flop	$Q^* = D$
JK flip-flop	$Q^* = \bar{K}Q + J\bar{Q}$
T flip-flop (edge-triggered)	$Q^* = \bar{Q}$
T flip-flop (clocked)	$Q^* = T\bar{Q} + \bar{T}Q$

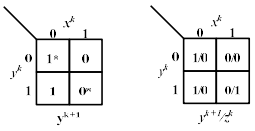


Figure 8.15

State Table and State Diagram for Example 8.4

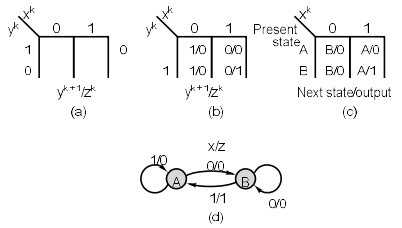


Figure 8.14

Timing Diagram for Example 8.4

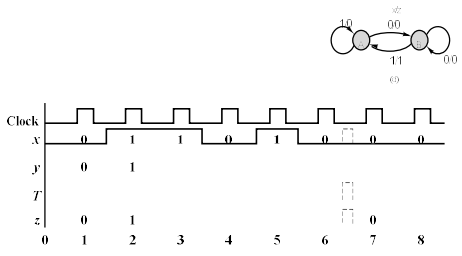


Figure 8.13

Timing Diagram for Example 8.4

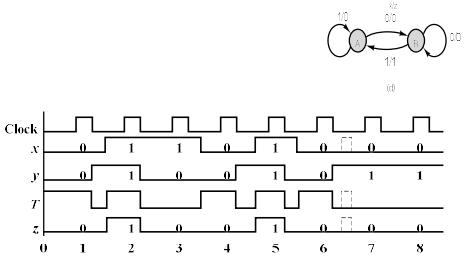
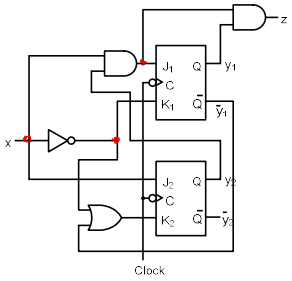


Figure 8.13

Synchronous Sequential Circuit with JK Flip-flops -- Example 8.5



$J_1 = xy_2$

$K_1 = \bar{x}$

$J_2 = x$

$K_2 = \bar{x} + \bar{y}_1$

$z = xy_1y_2$

Figure 8.16

K-Maps for Example 8.5

$J_1 = xy_2$

$K_1 = \bar{x}$

$J_2 = x$

$K_2 = \bar{x} + \bar{y}_1$

$z = xy_1y_2$

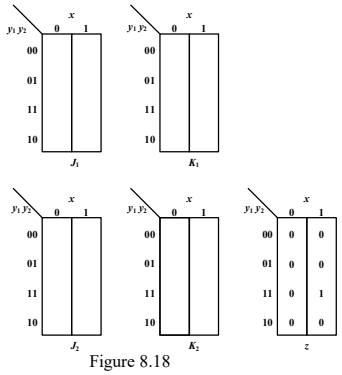


Figure 8.18

K-Maps for Example 8.5

$J_1 = xy_2$

$K_1 = \bar{x}$

$J_2 = x$

$K_2 = \bar{x} + \bar{y}_1$

$z = xy_1y_2$

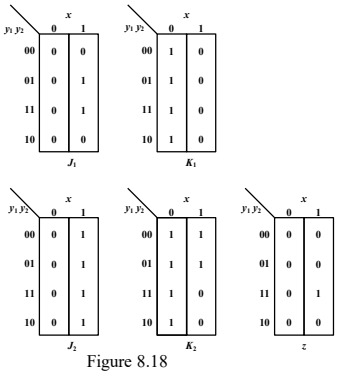
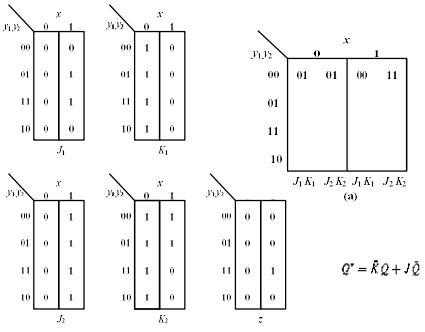


Figure 8.18

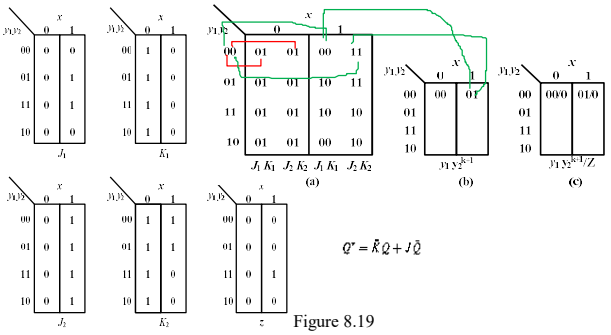
Generating the State Table From K-maps -- Example 8.5



$Q^+ = \bar{K}Q + J\bar{Q}$

Figure 8.19

Generating the State Table From K-maps -- Example 8.5



$Q^+ = \bar{K}Q + J\bar{Q}$

Figure 8.19

Generating the State Table From K-maps -- Example 8.5

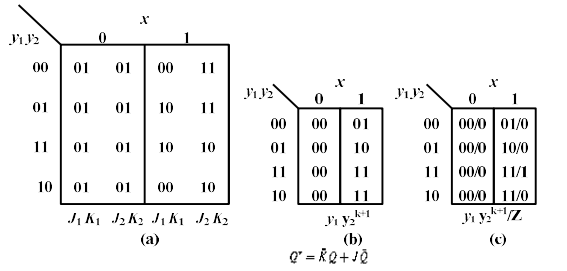


Figure 8.19

Timing Diagram and State Table for Example 8.5

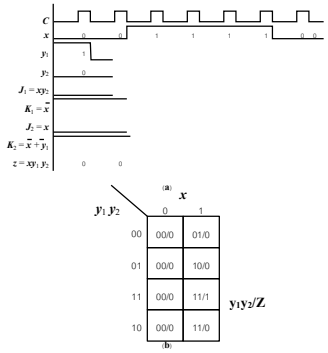


Figure 8.17

Timing Diagram and State Table for Example 8.5

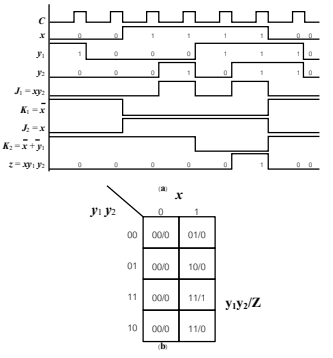


Figure 8.17

Synchronous Sequential Circuit Synthesis

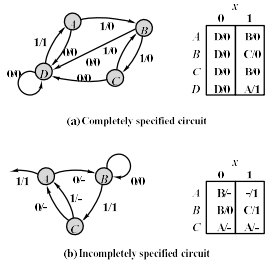


Figure 8.20

Flip-flop Input Tables -- Example 8.6

State transitions Q(t)	Q(t+e)	Required inputs D(t)
0	0	0
0	1	1
1	0	0
1	1	1

(a) D flip-flop

State transitions Q(t)	Q(t+e)	Required inputs S(t)	R(t)
0	0	0	d
0	1	1	0
1	0	0	1
1	1	d	0

(b) Clocked SR

State transitions Q(t)	Q(t+e)	Required inputs T(t)
0	0	0
0	1	1
1	0	1
1	1	0

(c) Clocked T flip-flop

State transitions Q(t)	Q(t+e)	Required inputs J(t)	K(t)
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

(d) Clocked JK flip-flop

TABLE 6.3 SUMMARY OF LATCH AND FLIP-FLOP CHARACTERISTICS

Device	Characteristic Equation
SR latch	$Q^* = S + \bar{R}Q$
Gated SR latch	$Q^* = SC + \bar{Q}R + \bar{C}Q$
D latch	$Q^* = DC + \bar{C}Q$
SR flip-flop	$Q^* = S + \bar{R}Q$
D flip-flop	$Q^* = D$
JK flip-flop	$Q^* = \bar{R}Q + J\bar{Q}$
T flip-flop (edge-triggered)	$Q^* = \bar{Q}$
T flip-flop (clocked)	$Q^* = T\bar{Q} + \bar{T}Q$

Figure 8.22

Flip-flop Input Tables -- Example 8.6

(a) D flip-flop

(b) Clocked SR

(c) Clocked T flip-flop

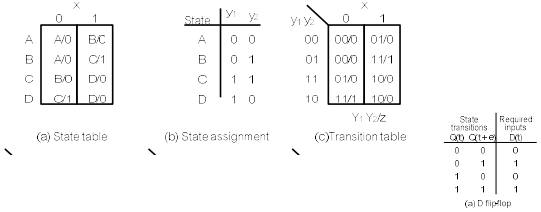
(d) Clocked JK flip-flop

TABLE 6.3 SUMMARY OF LATCH AND FLIP-FLOP CHARACTERISTICS

Device	Characteristic Equation
SR latch	$Q^* = S + \bar{R}Q$
Gated SR latch	$Q^* = SC + \bar{Q}R + \bar{C}Q$
D latch	$Q^* = DC + \bar{C}Q$
SR flip-flop	$Q^* = S + \bar{R}Q$
D flip-flop	$Q^* = D$
JK flip-flop	$Q^* = \bar{R}Q + J\bar{Q}$
T flip-flop (edge-triggered)	$Q^* = \bar{Q}$
T flip-flop (clocked)	$Q^* = T\bar{Q} + \bar{T}Q$

Figure 8.22

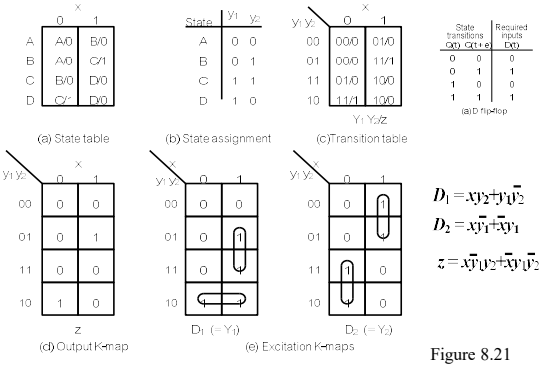
Introductory Synthesis Example -- Example 8.6



(a) State table (b) State assignment (c) Transition table (a) D flip-flop

Figure 8.21

Introductory Synthesis Example -- Example 8.6



(a) State table (b) State assignment (c) Transition table (a) D flip-flop

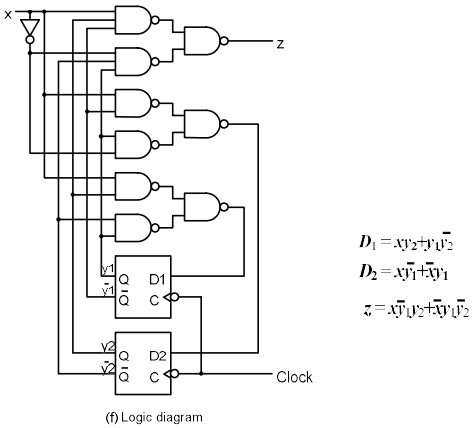
(d) Output K-map (e) Excitation K-maps

$D_1 = xy_2 + y_1\bar{y}_2$

$D_2 = x\bar{y}_1 + \bar{x}y_1$

$z = x\bar{y}_1y_2 + \bar{x}y_1\bar{y}_2$

Figure 8.21



$D_1 = xy_2 + y_1\bar{y}_2$

$D_2 = x\bar{y}_1 + \bar{x}y_1$

$z = x\bar{y}_1y_2 + \bar{x}y_1\bar{y}_2$

(f) Logic diagram

Generating the JK Flip-flop Excitation Maps -- Example 8.7

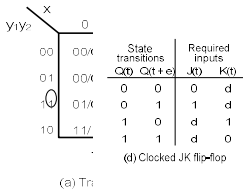


Figure 8.23

Generating the JK Flip-flop Excitation Maps -- Example 8.7

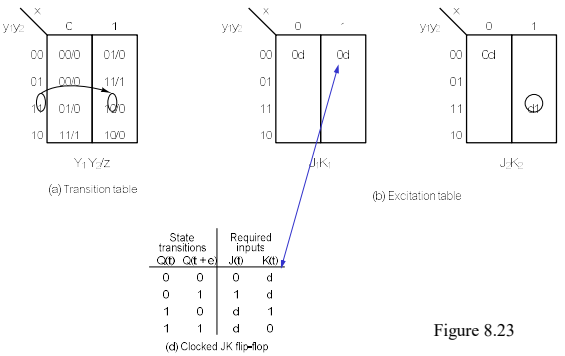


Figure 8.23

Generating the JK Flip-flop Excitation Maps -- Example 8.7

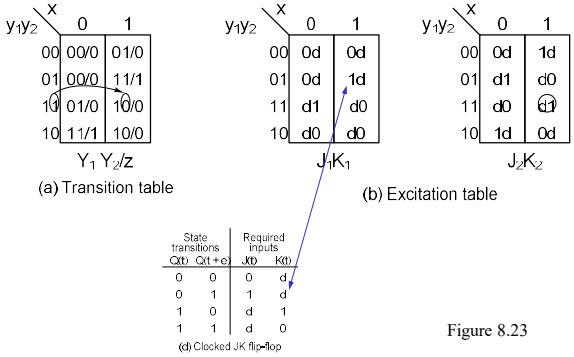


Figure 8.23

Generating the JK Flip-flop Excitation Maps --

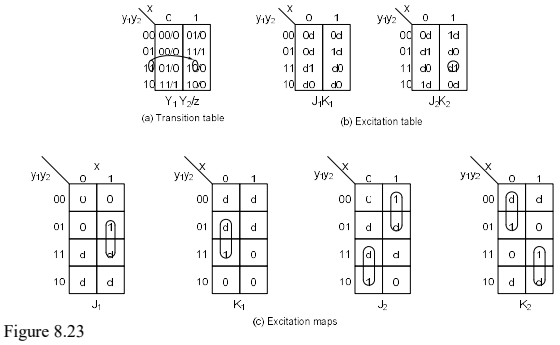


Figure 8.23

Clocked JK Flip-Flop Implementation -- Example 8.7

$J_1 = xy_2$

$K_1 = \bar{x}y_2$

$J_2 = x\bar{y}_1 + \bar{x}y_1$

$K_2 = \bar{x}\bar{y}_1 + xy_1$

$z = xy_1\bar{y}_2 + \bar{x}y_1\bar{y}_2$

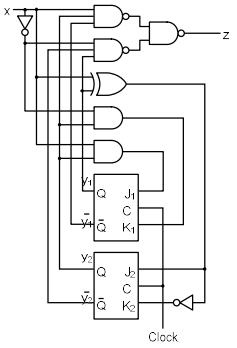


Figure 8.24

Application Equation Method for Deriving Excitation Equations -- Example 8.8

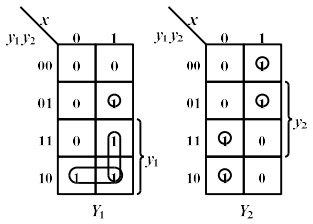


Figure 8.25

Sequence Recognizer for 01 Sequence -- Example 8.9

x = 010100000111101

Z = 010100000100001

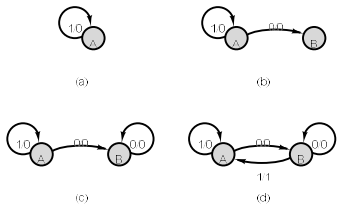


Figure 8.26

Synthesis of the 01 Recognizer with SR Flip-flops

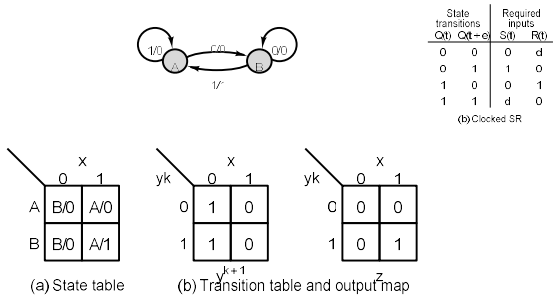
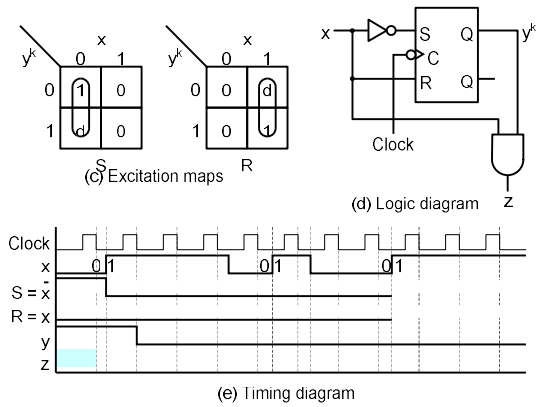
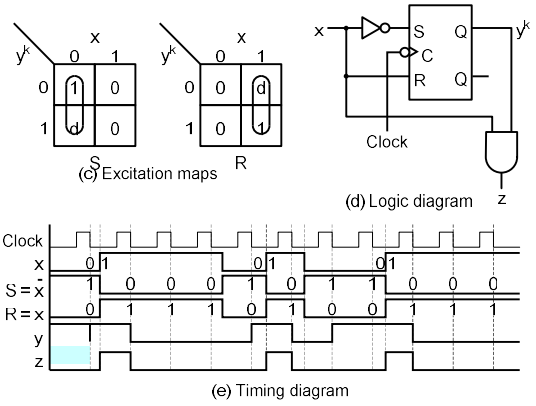


Figure 8.27





Realization of 01 Recognizer with T Flip-flops and JK flip-flops

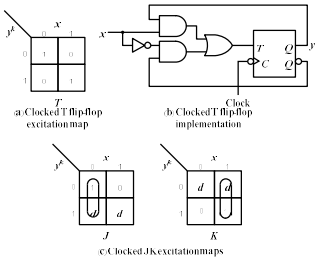


Figure 8.28

Design of a Recognizer for the Sequence 1111 -- Example 8.11

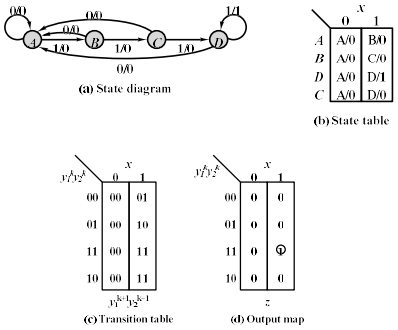


Figure 8.29

SR Realization of the 1111 Recognizer

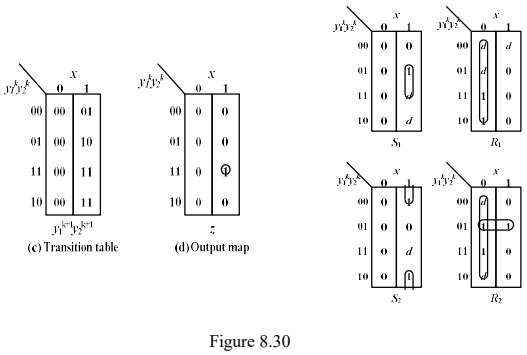


Figure 8.30

Clocked T and JK Realizations of the 1111 Recognizer

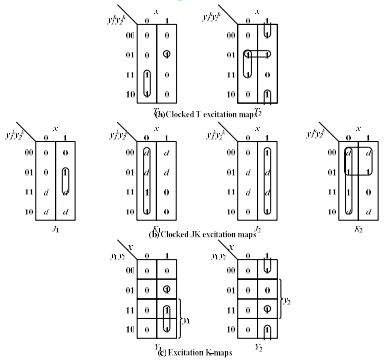


Figure 8.31

Clocked JK Flip-Flop Realization of a 1111 Recognizer

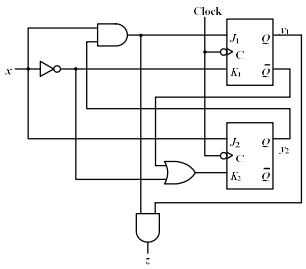
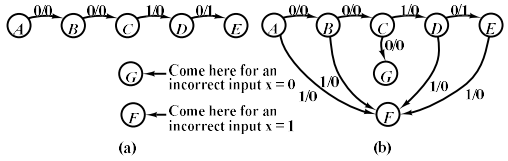


Figure 8.32

Design of a 0010 Recognizer



X=010110010010

Figure 8.33

Design of a 0010 Recognizer

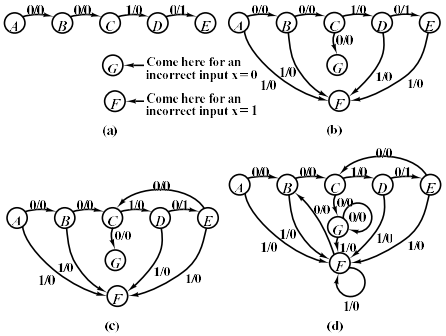


Figure 8.33

Design of a 0010 Recognizer

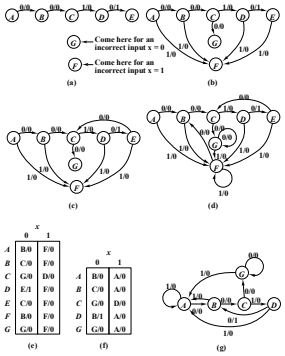


Figure 8.33

Design of a Serial Binary Adder

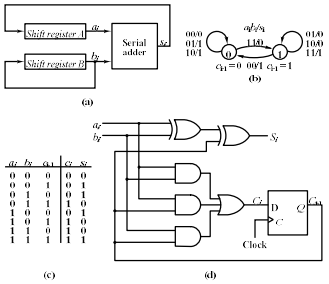
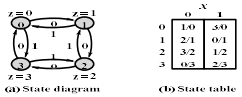


Figure 8.34

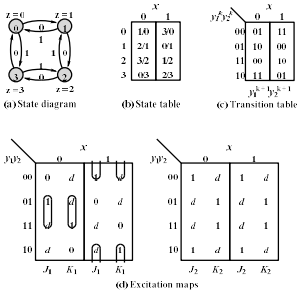
Design of a Four-State Up/Down Counter



(a) State diagram (b) State table

Figure 8.35

Design of a Four-State Up/Down Counter



(a) State diagram (b) State table (c) Transition table

(d) Excitation maps

Figure 8.35

An Implementation of the Up/Down Counter

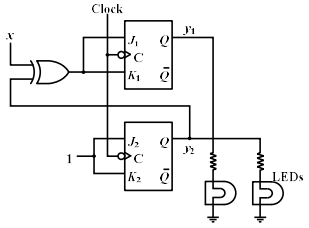


Figure 8.36