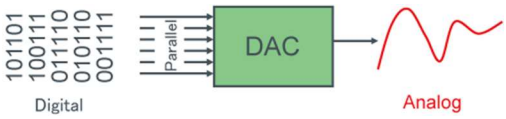
A/D Converter and D/A Converter

- **D/A Converters**
- D/A converters convert digital signals into analog format.



Digital Data:
Evenly spaced discontinuous values
Temporally discrete, quantitatively discrete
Analog Data (Natural Phenomena):
Continuous range of values
Temporally continuous, quantitatively continuous

A/D Converter and D/A Converter

- **A/D Converters**
- An A/D converter is a device that converts analog signals (usually voltage) obtained from environmental (physical) phenomena into digital format
- Conversion involves a series of steps, including sampling, quantization, and coding.

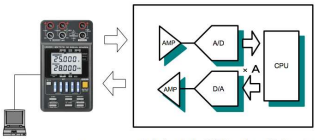
A/D Converter and D/A Converter

A/D Converter Applications

Digital Audio:
Digital audio workstations, sound recording, pulse-code modulation
Digital signal processing:
TV tuner cards, microcontrollers, digital storage oscilloscopes
Scientific instruments:
Digital imaging systems, radar systems, temperature sensors

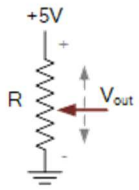
D/A Converter Applications

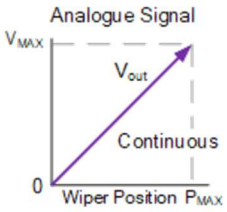
Digital Audio：
CD, MD, 1-bit Audio
Digital Video：
DVD, Digital Still Camera
Communication Equipment：
Smartphones, FAX, ADSl equipment
PCs：
Audio, video cards
Measurement instruments：
Programmable power supplies, etc.

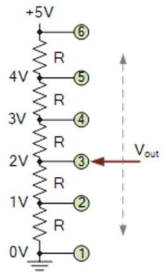


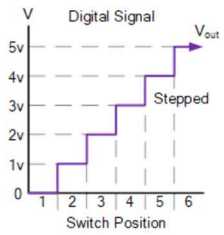
DC SIGNAL SOURCE SS7012 Evaluation circuit of A/D Converter → D/A Converter

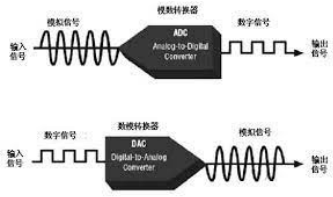
Analogue and Digital Signals



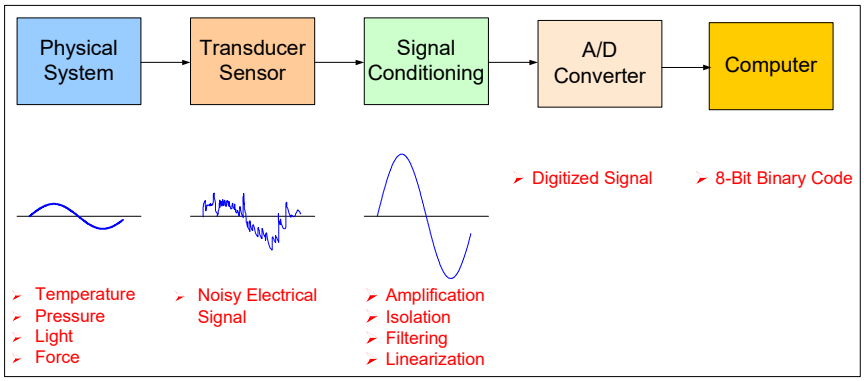








Analog to Digital (A/D) Converter

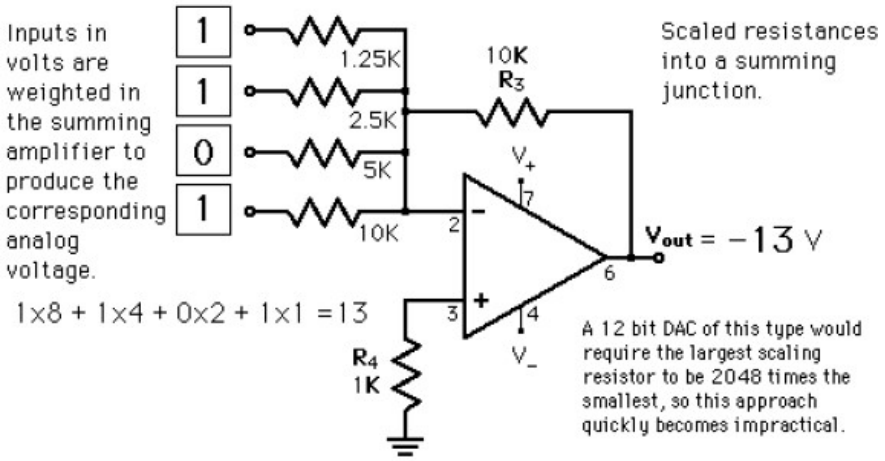


- Input signal
- Sampling rate
- Throughput
- Resolution
- Range
- Gain

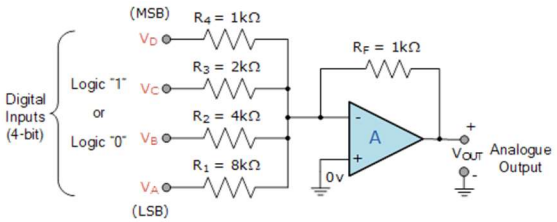
Digital-to-Analog Conversion

- When data is in binary form, the 0's and 1's may be of several forms such as the TTL form where the logic zero may be a value up to 0.8 volts and the 1 may be a voltage from 2 to 5 volts. The data can be converted to clean digital form using gates which are designed to be on or off depending on the value of the incoming signal. Data in clean binary digital form can be converted to an analog form by using a summing amplifier. For example, a simple 4-bit D/A converter can be made with a four-input summing amplifier. More practical is the R-2R Network DAC.

Four-Bit D/A Converter



Inverting Summing Amplifier Circuit

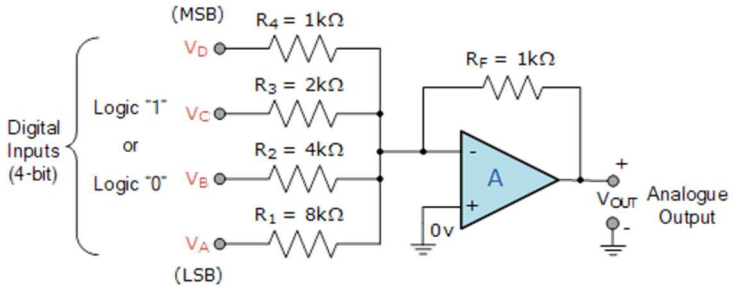


$$I_F = I_1 + I_2 + I_3 + I_4 = \frac{V_{IN1}}{R_1} + \frac{V_{IN2}}{R_2} + \frac{V_{IN3}}{R_3} + \frac{V_{IN4}}{R_4}$$

$$V_{OUT} = \frac{R_F}{R_{IN}} \times V_{IN} = -\left(\frac{R_F}{R_1}V_{IN1} + \frac{R_F}{R_2}V_{IN2} + \frac{R_F}{R_3}V_{IN3} + \frac{R_F}{R_4}V_{IN4}\right)$$

$$\therefore V_{OUT} = -\frac{R_F}{R_{IN}}\left(V_{IN1} + V_{IN2} + V_{IN3} + V_{IN4}\right)$$

Inverting Summing Amplifier Circuit

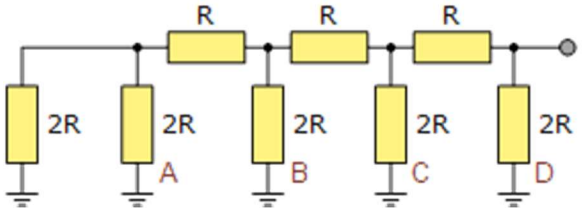


$$V_{OUT} = -\left[\frac{R_F}{R_4}V_D + \frac{R_F}{R_3}V_C + \frac{R_F}{R_2}V_B + \frac{R_F}{R_1}V_A\right]$$

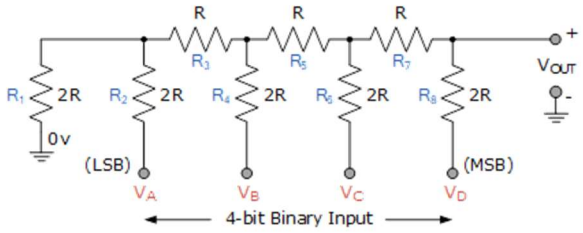
$$V_{OUT} = -\left[\frac{1k\Omega}{1k\Omega}V_D + \frac{1k\Omega}{2k\Omega}V_C + \frac{1k\Omega}{4k\Omega}V_B + \frac{1k\Omega}{8k\Omega}V_A\right]$$

$$V_{OUT} = -\left[1V_D + \frac{1}{2}V_C + \frac{1}{4}V_B + \frac{1}{8}V_A\right]$$

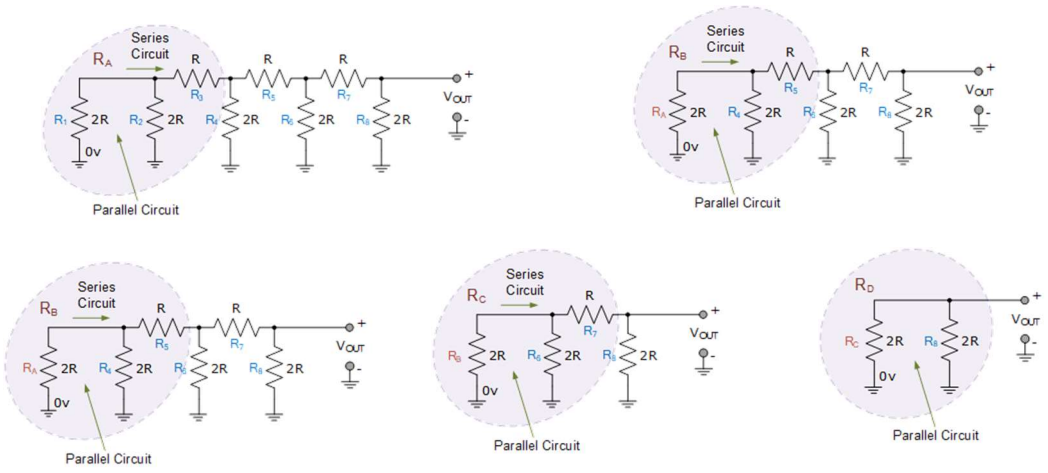
4-bit R-2R Resistive Ladder Network



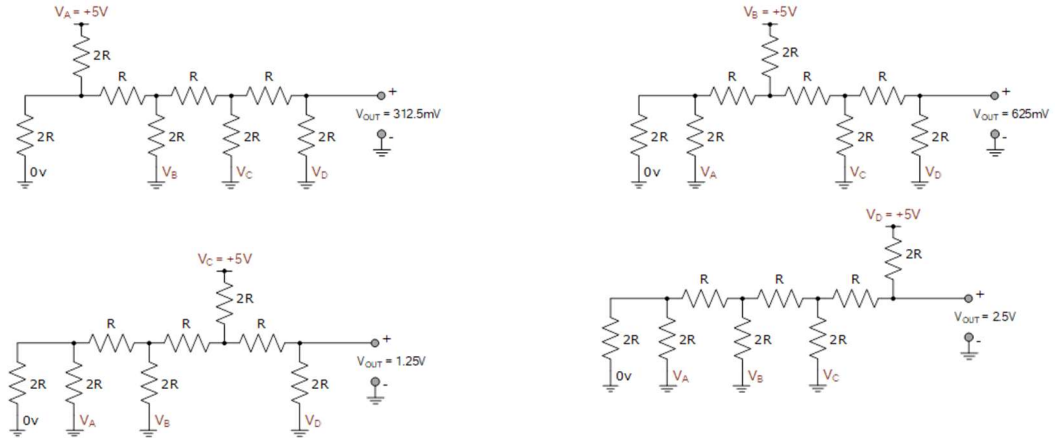
$$V_{OUT} = \frac{V_A + 2V_B + 4V_C + 8V_D + 16V_E + 32V_F + \ldots etc}{2^n}$$



4-bit R-2R Resistive Ladder Network

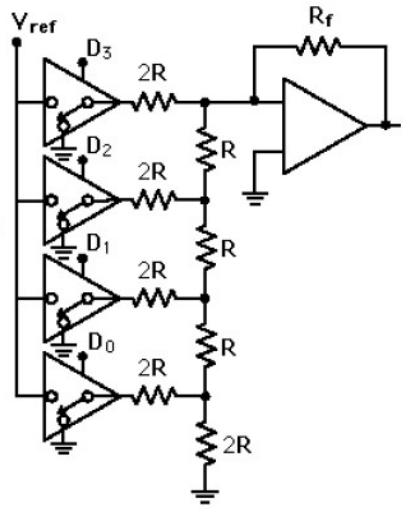


4-bit R-2R Resistive Ladder Network



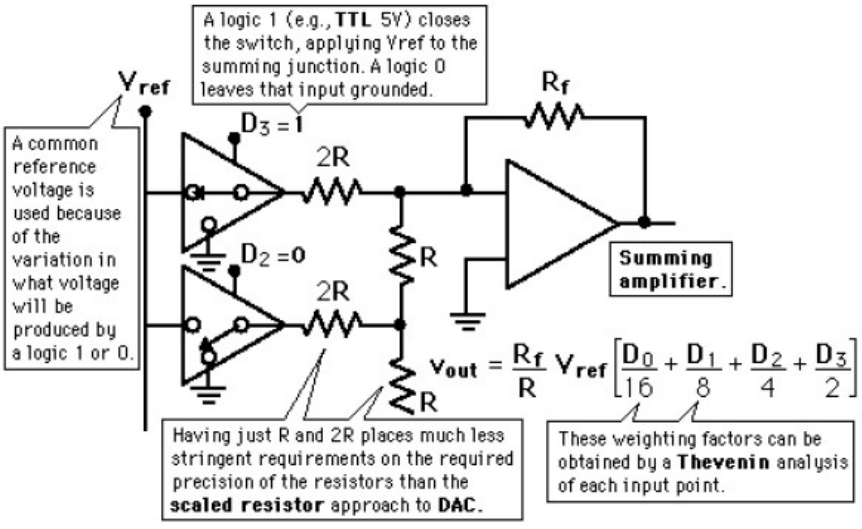
$$V_{OUT} = \frac{V_A + 2V_B + 4V_C + 8V_D}{16}$$

R-2R Ladder DAC

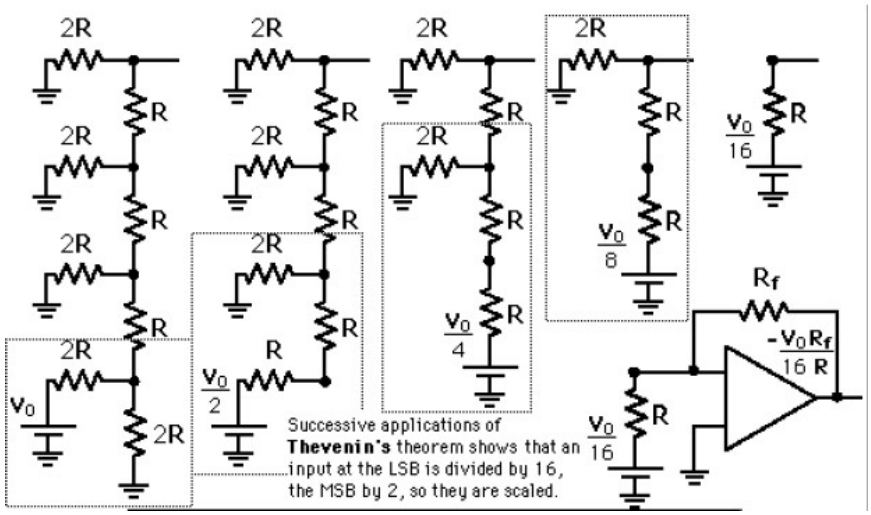


$$v_{out} = \frac{R_f}{R} V_{ref}\left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2}\right]$$

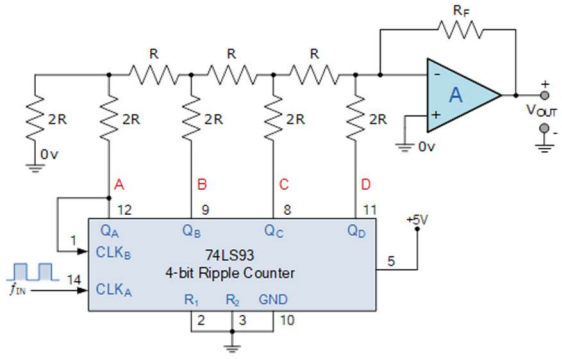
R-2R Ladder DAC Details

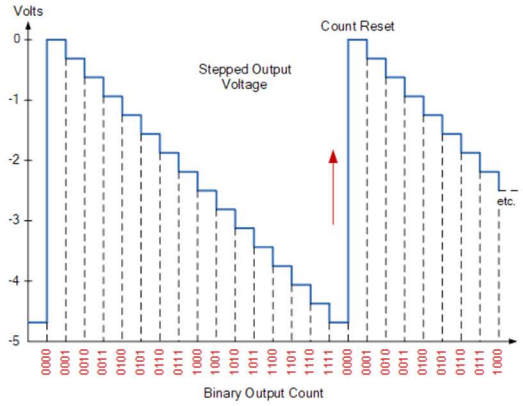


Thevenin Example: R-2R Ladder



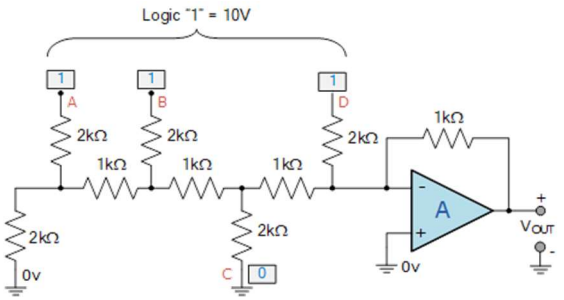
4-bit Binary Counting R-2R DAC





4-bit R-2R DAC Timing Diagram

R-2R D/A Converter Example



$$V_{OUT} = \frac{1V_A + 2V_B + 4V_C + 8V_D}{2^n}$$

$$V_{OUT} = \frac{1\times10 + 2\times10 + 4\times0 + 8\times10}{16}$$

$$V_{OUT} = \frac{110}{16} = 6.875 \text{ Volts}$$

$$\text{Resolution} = V_{(LSB)} = \frac{V_{IN}}{2^n}$$

$$\therefore \text{Resolution} = \frac{10}{16} = 0.625 \text{ Volts}$$

Unipolar Code

Base 10 number	SCALE	+ 10V FS	BANARY	GRAY
+15	+FS - 1LSB = +15/16 FS	9.375	1 1 1 1	1 0 0 0
+14	+7/8 FS	8.750	1 1 1 0	1 0 0 1
+13	+13/16 FS	8.125	1 1 0 1	1 0 1 1
+12	+3/4 FS	7.500	1 1 0 0	1 0 1 0
+11	+11/16 FS	6.875	1 0 1 1	1 1 1 0
+10	+5/8 FS	6.250	1 0 1 0	1 1 1 1
+9	+9/16 FS	5.625	1 0 0 1	1 1 0 1
+8	+1/2 FS	5.000	1 0 0 0	1 1 0 0
+7	+7/16 FS	4.375	0 1 1 1	0 1 0 0
+6	+3/8 FS	3.750	0 1 1 0	0 1 0 1
+5	+5/16 FS	3.125	0 1 0 1	0 1 1 1
+4	+1/4 FS	2.500	0 1 0 0	0 1 1 0
+3	+3/16 FS	1.875	0 0 1 1	0 0 1 0
+2	+1/8 FS	1.250	0 0 1 0	0 0 1 1
+1	1LSB = +1/16 FS	0.625	0 0 0 1	0 0 0 1
0	0	0.000	0 0 0 0	0 0 0 0

Bipolar Codes

Base 10 number	SCALE	± 5V FS	OFFSET BANARY	TWOS COMP.	ONES COMP.	SIGN MAG.
+7	+FS - 1LSB = +7/8 FS	+4.375	1 1 1 1	0 1 1 1	0 1 1 1	0 1 1 1
+6	+3/4 FS	+3.750	1 1 1 0	0 1 1 0	0 1 1 0	0 1 1 0
+5	+5/8 FS	+3.125	1 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1
+4	+1/2 FS	+2.500	1 1 0 0	0 1 0 0	0 1 0 0	0 1 0 0
+3	+3/8 FS	+1.875	1 0 1 1	0 0 1 1	0 0 1 1	0 0 1 1
+2	+1/4 FS	+1.250	1 0 1 0	0 0 1 0	0 0 1 0	0 0 1 0
+1	+1/8 FS	+0.625	1 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1
0	0	0.000	1 0 0 0	0 0 0 0	*0 0 0 0	*1 0 0 0
-1	-1/8 FS	-0.625	0 1 1 1	1 1 1 1	1 1 1 0	1 0 0 1
-2	-1/4 FS	-1.250	0 1 1 0	1 1 1 0	1 1 0 1	1 0 1 0
-3	-3/8 FS	-1.875	0 1 0 1	1 1 0 1	1 1 0 0	1 0 1 1
-4	-1/2 FS	-2.500	0 1 0 0	1 1 0 0	1 0 1 1	1 1 0 0
-5	-5/8 FS	-3.125	0 0 1 1	1 0 1 1	1 0 1 0	1 1 0 1
-6	-3/4 FS	-3.750	0 0 1 0	1 0 1 0	1 0 0 1	1 1 1 0
-7	-FS + 1LSB = -7/8 FS	-4.375	0 0 0 1	1 0 0 1	1 0 0 0	1 1 1 1
-8	-FS	-5.000	0 0 0 0	1 0 0 0		

NOT NORMALLY USED IN COMPUTATIONS

	ONES COMP.	TWOS COMP.
0+	0 0 0 0	1 0 0 0
* 0-	1 1 1 1	1 0 0 0

Quantization: The Size of a Least Significant Bit (LSB)

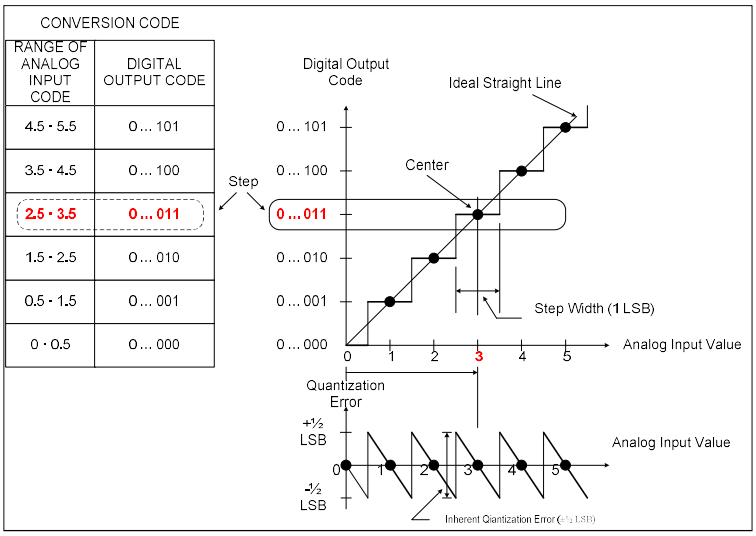
Resolution N	2^N	VOLTAGE (10V FS)	ppm FS	% FS	dB FS
2-bit	4	2.5V	250.000	25	-12
4-bit	16	625mV	62.500	6.25	-24
6-bit	64	156mV	15.625	1.56	-36
8-bit	256	39.1mV	3.906	0.39	-48
10-bit	1.024	9.77mV (10mV)	977	0.098	-60
12-bit	4.096	2.44mV	244	0.024	-72
14-bit	16.384	610µV	61	0.0061	-84
16-bit	65.536	153µV	15	0.0015	-96
18-bit	262.144	38µV	4	0.0004	-108
20-bit	1.048.576	9.54µV (10µV)	1	0.001	-120
22-bit	4.194.304	2.38µV	0.24	0.000024	-132
24-bit	16.777.216	596nV*	0.06	0.000006	-144

The resolution of data converters

$$1\ LSB = \frac{FSR}{(2^n - 1)} \quad for\ n-bit\ converter$$

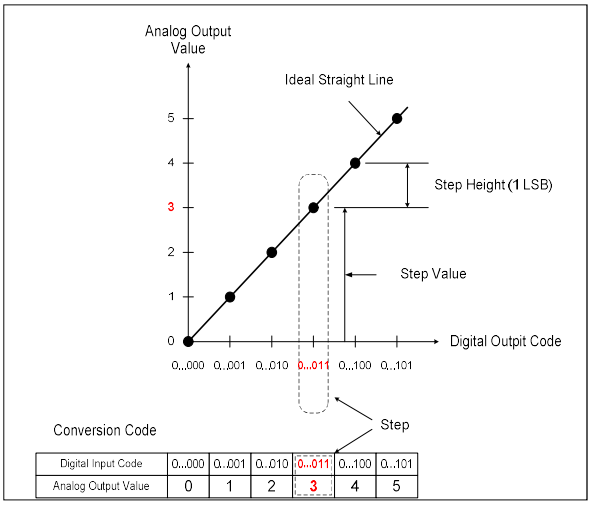
The Ideal Transfer Function (ADC)

The theoretical ideal transfer function for an ADC is a straight line, however, the practical ideal transfer function is a uniform staircase characteristic shown in Figure .



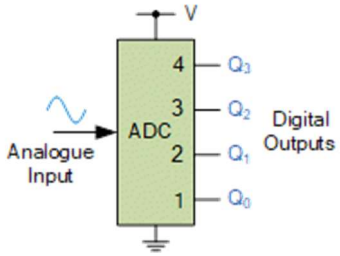
The Ideal Transfer Function (DAC)

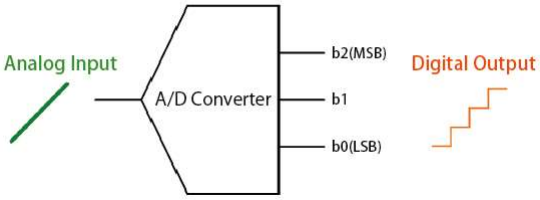
The DAC theoretical ideal transfer function would also be a straight line with an infinite number of steps but practically it is a series of points that fall on the ideal straight line as shown in Figure



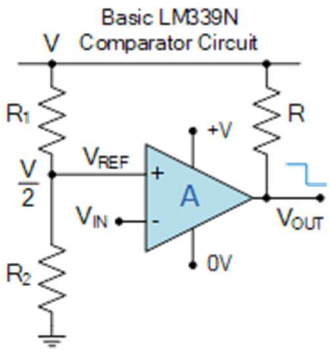
Analogue to Digital Converter

- Analogue to Digital Converter, or ADC, is a data converter which allows digital circuits to interface with the real world by encoding an analogue signal into a binary code

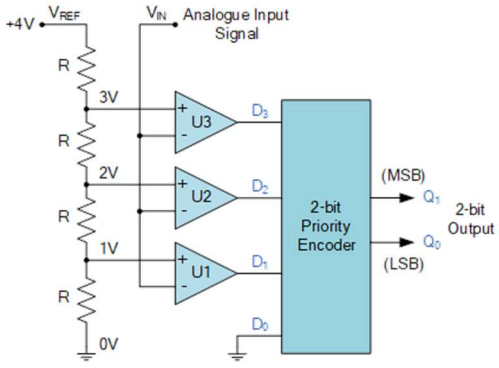




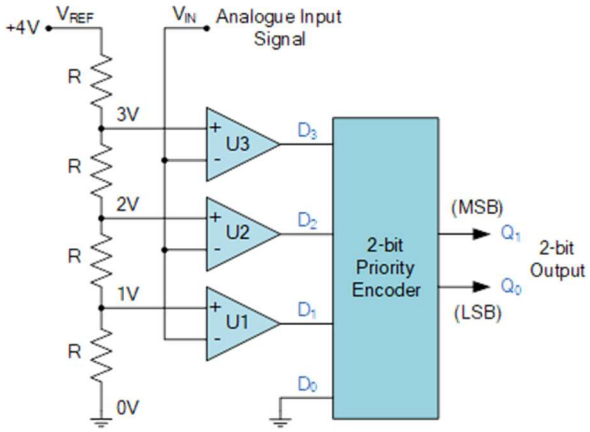
Comparator Circuit



2-bit Analogue to Digital Converter Circuit



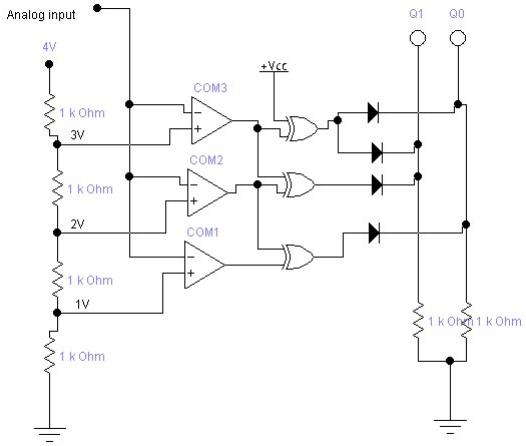
2-bit Analogue to Digital Converter Circuit



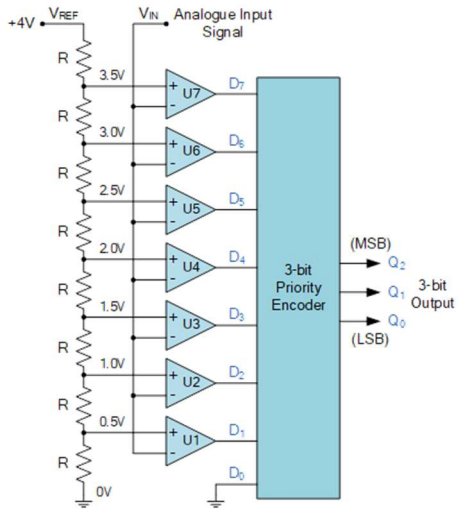
Analogue Input Voltage (V_{IN})	Comparator Outputs				Digital Outputs	
	D_3	D_2	D_1	D_0	Q_1	Q_0
0 to 0.99 V	1	1	1	**0**	0	0
1 to 1.99 V	1	1	**0**	X	0	1
2 to 2.99 V	1	0	X	X	1	0
3 to 4 V	**0**	X	X	X	1	1

Where: "X" is a "don't care", that is either a logic "0" or a logic "1" condition.

2-bit ADC Using Diodes

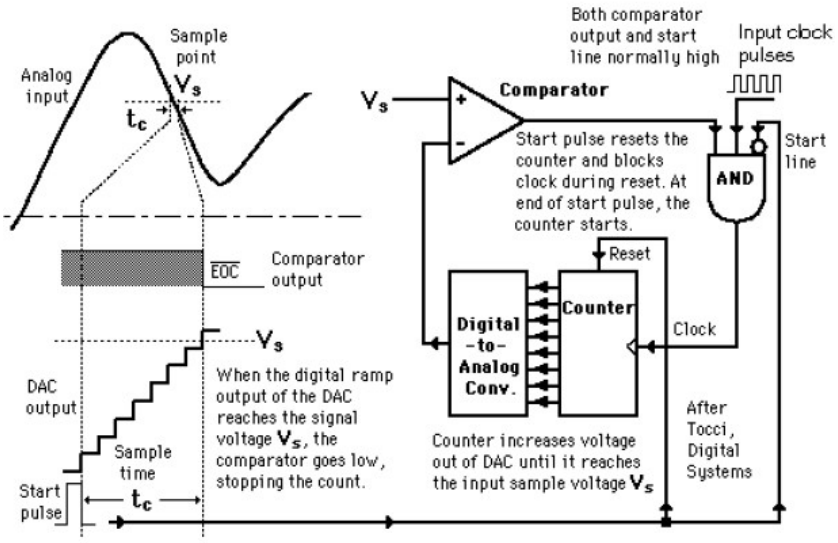


3-bit Analogue to Digital Converter Circuit

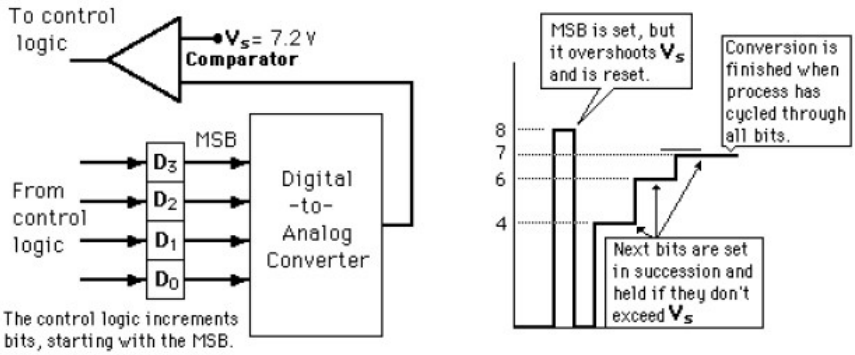


Analogue Input Voltage (V_{IN})	Comparator Outputs								Digital Outputs		
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0 to 0.49 V	1	1	1	1	1	1	1	**0**	0	0	0
0.5 to 0.99 V	1	1	1	1	1	1	**0**	X	0	0	1
1.0 to 1.49 V	1	1	1	1	1	0	X	X	0	1	0
1.5 to 1.99 V	1	1	1	1	**0**	X	X	X	0	1	1
2.0 to 2.49 V	1	1	1	**0**	X	X	X	X	1	0	0
2.5 to 2.99 V	1	1	**0**	X	X	X	X	X	1	0	1
3.0 to 3.49 V	1	**0**	X	X	X	X	X	X	1	1	0
3.5 to 4.0 V	**0**	X	X	X	X	X	X	X	1	1	1

Digital Ramp ADC



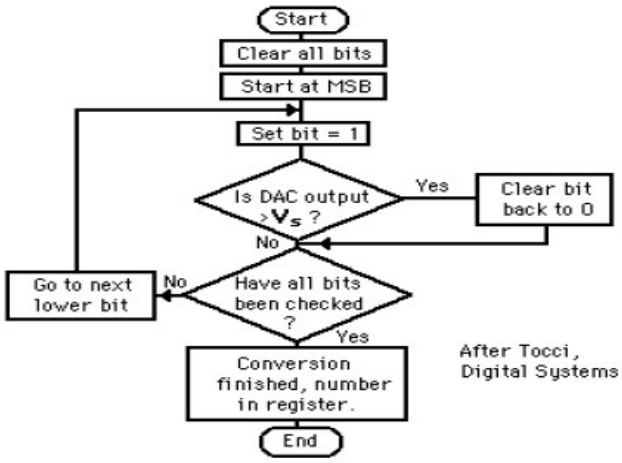
Successive Approximation ADC



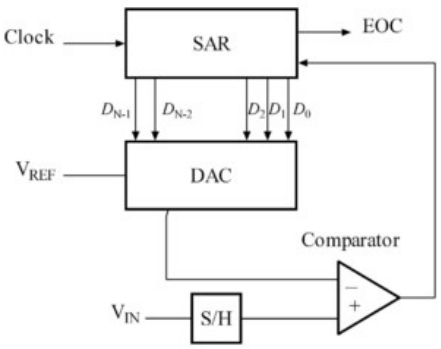
Successive Approximation ADC

- The successive approximation ADC is much faster than the digital ramp ADC because it uses digital logic to converge on the value closest to the input voltage. A comparator and a DAC are used in the process.

Successive Approximation ADC

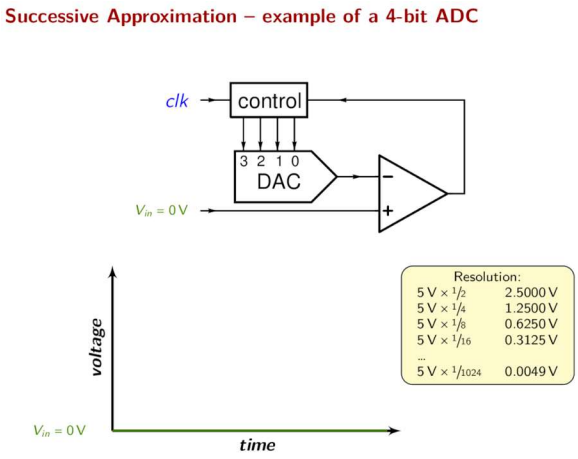


Successive-approximation ADC

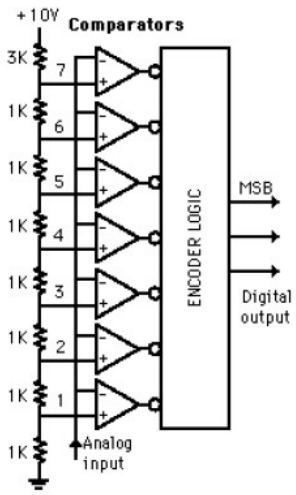


DAC = digital-to-analog converter
EOC = end of conversion
SAR = successive approximation register
S/H = sample and hold circuit
VIN = input voltage
VREF = reference voltage

Successive-approximation ADC



Flash ADC



Illustrated is a 3-bit flash ADC with resolution 1 volt (after Tocci). The resistor net and comparators provide an input to the combinational logic circuit, so the conversion time is just the propagation delay through the network - it is not limited by the clock rate or some convergence sequence. It is the fastest type of ADC available, but requires a comparator for each value of output (63 for 6-bit, 255 for 8-bit, etc.) Such ADCs are available in IC form up to 8-bit and 10-bit flash ADCs (1023 comparators) are planned. The encoder logic executes a truth table to convert the ladder of inputs to the binary number output.

Caracteristics ADC

SYSTEM ARCHITECTURE	RESOLUTION	SPEED	ADVANTAGE / DRAWBACKS
Flash	8 bits	250MSPS – 1GSPS	+ Extremly fast + High input bandwidth - Higher power consumption - Large die size - High input capacitance - Expansive - Sparkle codes
SAR	10 bits – 16 bits	76kSPS – 250kSPS	+ High resolution and accuracy + Low power consumption + Fev external components - Low input bandwidth - Limited sampling rate - V_{IN} must retain constant during conv.
Integrating	> 18 bits	< 50 kSPS	+ High resolution + Low supplay current + Excelant noise rejection - Low speed
Sigma-Delta (Σ–Δ)	> 16 bits	> 200 kSPS	+ High resolution + High input bandwidth + Digital on-chip filtering - External T/H - Limited sampling rate
Pipeline	12 bits – 16 bits	1MSPS – 80MSPS	+ High throughtput rate + Low power consumption + Digital error correction and on-chip self- calibration - Required duty-cycle typical - Required minimum clock frequency