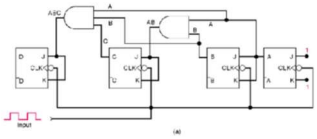
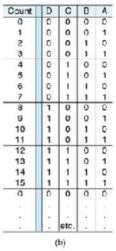
7-6 Synchronous (Parallel) counters

- Synchronous (parallel) counters
  - All of the FFs are triggered simultaneously by the clock input pulses.
  - Overcome the problem caused by FF propagation delay.



35

Circuit operation



Only those FFs that are supposed to toggle on that NGT should have J=K=1 when that NGT occurs.

36

Synchronous Counter

คุณสมบัติของ JK FF		
J	K	Q
0	0	No Change
0	1	0
1	0	1
1	1	Toggle

สถานะของเอ้าท์พุท			
$Q_{เดิม}$	$Q_{ใหม่}$	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

37

Synchronous Counter Modulo 6

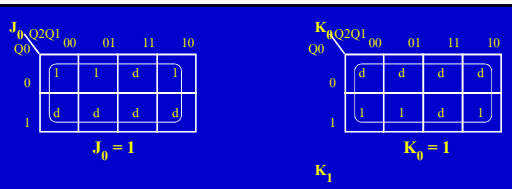
CP	Q_2	Q_1	Q_0	J_0	K_0	J_1	K_1	J_2	K_2
0	0	0	0	1		0	d		
1	0	0	1						
2	0	1	0						
3	0	1	1						
4	1	0	0						
5	1	0	1						
6	0	0	0						

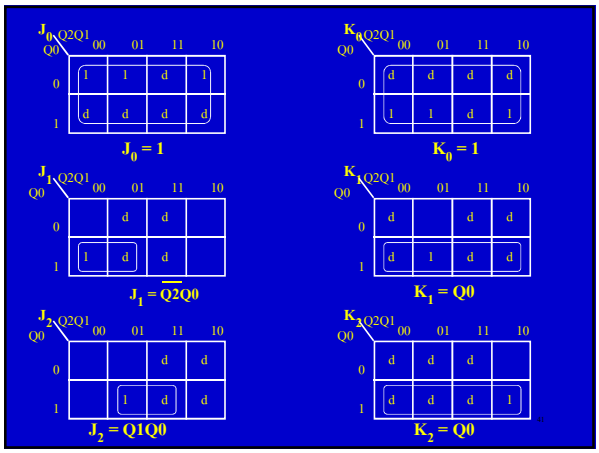
38

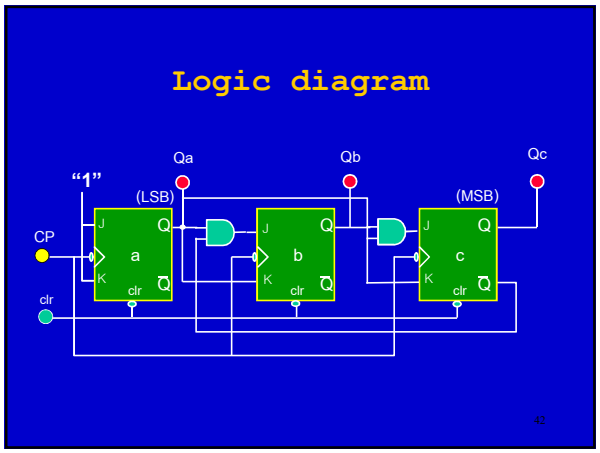
Synchronous Counter Modulo 6

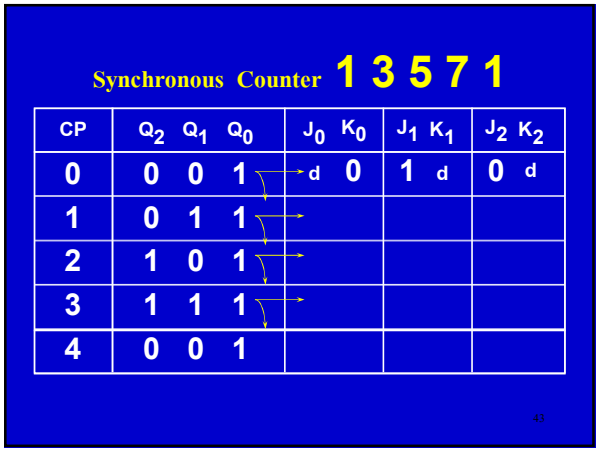
CP	Q_2	Q_1	Q_0	J_0	K_0	J_1	K_1	J_2	K_2
0	0	0	0	1	d	0	d	0	d
1	0	0	1	d	1	1	d	0	d
2	0	1	0	1	d	d	0	0	d
3	0	1	1	d	1	d	1	1	d
4	1	0	0	1	d	0	d	d	0
5	1	0	1	d	1	0	d	d	1
6	0	0	0						

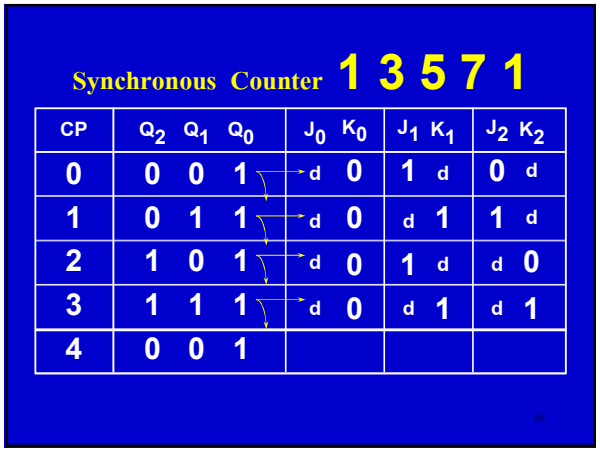
39

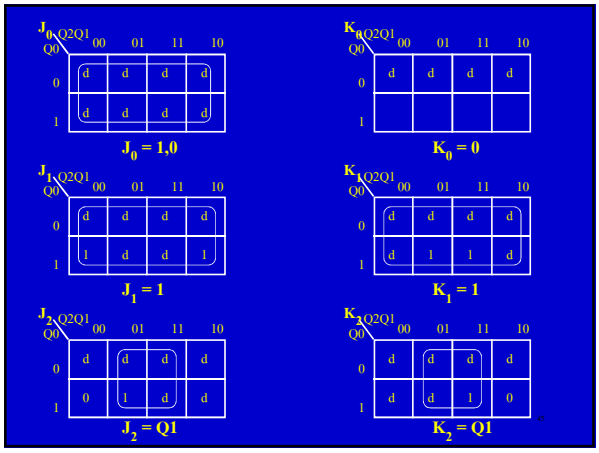


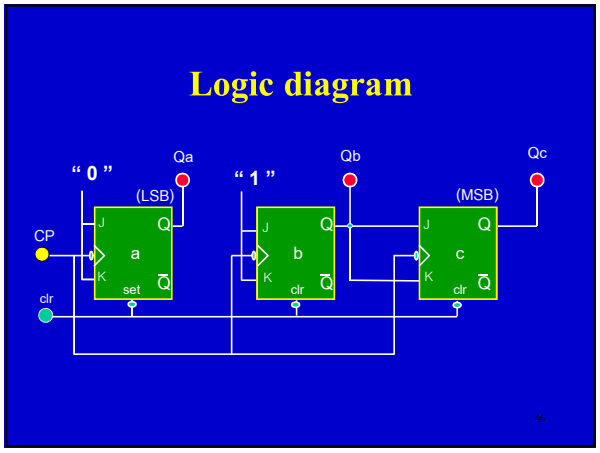

J_0 Q2Q1 / Q0 00 01 11 10 / 0: 1 1 d 1 / 1: d d d d
$J_0 = 1$
K_0 Q2Q1 / Q0 00 01 11 10 / 0: d d d d / 1: 1 1 d 1
$K_0 = 1$
J_1 Q2Q1 / Q0 00 01 11 10 / 0: d d / 1: 1 d d
$J_1 = \overline{Q2}Q0$
K_1 Q2Q1 / Q0 00 01 11 10 / 0: d d d / 1: d 1 d d
$K_1 = Q0$
J_2 Q2Q1 / Q0 00 01 11 10 / 0: d d / 1: 1 d d
$J_2 = Q1Q0$
K_2 Q2Q1 / Q0 00 01 11 10 / 0: d d d / 1: d d d 1
$K_2 = Q0$


Logic diagram
"1"
Qa
Qb
Qc
(LSB)
(MSB)
CP
clr
J
K
Q
a
b
c
clr
42

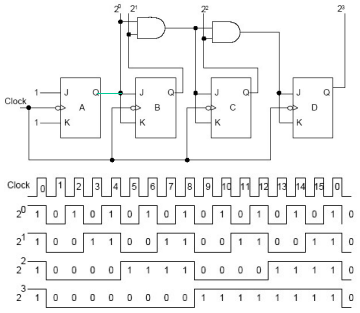

Synchronous Counter 1 3 5 7 1
CP | Q_2 Q_1 Q_0 | J_0 K_0 | J_1 K_1 | J_2 K_2
0 | 0 0 1 | d 0 | 1 d | 0 d
1 | 0 1 1 | | |
2 | 1 0 1 | | |
3 | 1 1 1 | | |
4 | 0 0 1 | | |
43


Synchronous Counter 1 3 5 7 1
CP | Q_2 Q_1 Q_0 | J_0 K_0 | J_1 K_1 | J_2 K_2
0 | 0 0 1 | d 0 | 1 d | 0 d
1 | 0 1 1 | d 0 | d 1 | 1 d
2 | 1 0 1 | d 0 | 1 d | d 0
3 | 1 1 1 | d 0 | d 1 | d 1
4 | 0 0 1 | | |
44

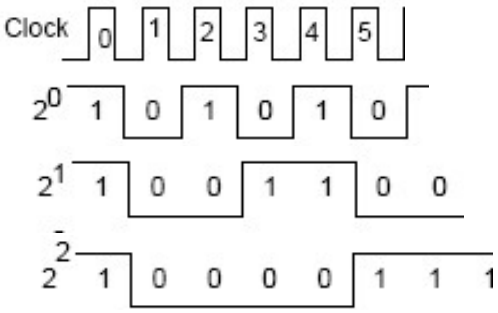

J_0 Q2Q1 / Q0 00 01 11 10 / 0: d d d d / 1: d d d d
$J_0 = 1,0$
K_0 Q2Q1 / Q0 00 01 11 10 / 0: d d d d / 1:
$K_0 = 0$
J_1 Q2Q1 / Q0 00 01 11 10 / 0: d d d d / 1: 1 d d 1
$J_1 = 1$
K_1 Q2Q1 / Q0 00 01 11 10 / 0: d d d d / 1: d 1 1 d
$K_1 = 1$
J_2 Q2Q1 / Q0 00 01 11 10 / 0: d d d d / 1: 0 1 d d
$J_2 = Q1$
K_2 Q2Q1 / Q0 00 01 11 10 / 0: d d d d / 1: d d 1 0
$K_2 = Q1$


Logic diagram
" 0 "
" 1 "
Qa
Qb
Qc
(LSB)
(MSB)
CP
clr
J
K
Q
a
b
c
set
clr
46

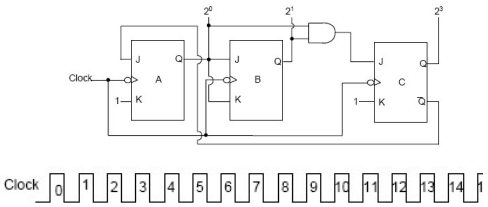
วงจรนับแบบซิงโครนัส (Synchronous Counter)



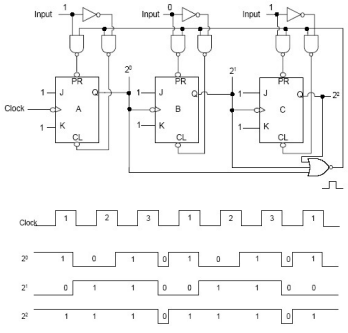
47



วงจรนับแบบซิงโครนัส หาร .....(Synchronous Counter)



49



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Advantage of Synchronous counters over Asychronous

- States are changed simultaneously.
  - Total delay
    - FFt_{pd}+ANDgate t_{pd}
- Actual Ics
  - 74ALS160/162, 74HC160/162: Synchronous decade counters
  - 74ALS161/163, 74HC161/163: Synchronous MOD-16 counters

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Example

- Determine f_{max} for the counter of Figure 7-17(a) if t_{pd} for each FF is 50ns and t_{pd} for each AND gate is 20 ns. Compare this value with f_{max} for a MOD-16 ripple counter.
- What must be done to convert this counter to MOD-32?
- Determine f_{max} for the MOD-32 parallel counter.

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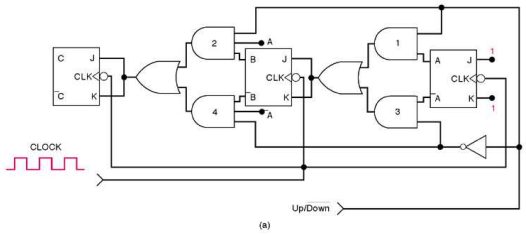
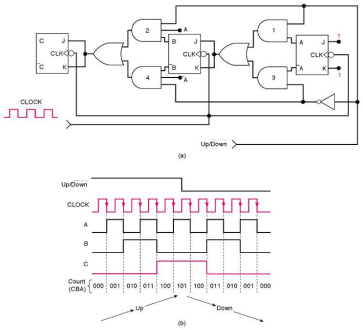
Review Questions

- What is the advantage of a synchronous counter over an asynchronous counter? What is the disadvantage?
- How many logic devices are required for a MOD-64 parallel counter?
- What logic signal drives the J,K inputs of the MSB flip-flop for the counter of question 2?

7-7 Synchronous Down and UP/Down counters



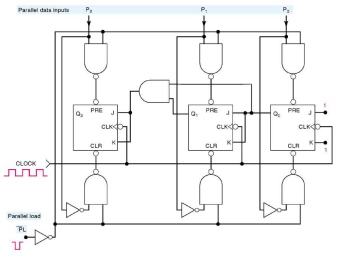
7-7 Synchronous Down and UP/Down counters



Example

- What problems might be caused if the UP/Down signal changes levels on the NGT of the clock?

Presettable counters



Synchronous Presetting

- Examples of IC counters
  - 74ALS160, 74ALS161, 74ALS612, 74ALS163
  - 74Hc160, 74HC161, 74HC162, 74HC163

Review Questions

- **What is meant when we say that a counter is presettable?**
- **Describe the difference between asynchronous and synchronous presetting.**

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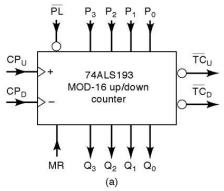
The 74ALS193/HC193



(a)

Pin	Description
CP_U	Count-up clock input (active rising edge)
CP_D	Count-down clock input (active rising edge)
MR	Asynchronous master reset input (active HIGH)
$\overline{PL}$	Asynchronous parallel load input (active LOW)
P_0-P_3	Parallel data inputs
Q_0-Q_3	Flip-flop outputs
$\overline{TC}_D$	Terminal count-down (borrow) output (active LOW)
$\overline{TC}_U$	Terminal count-up (carry) output (active) LOW

(b)

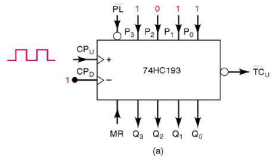
Mode Select

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Asynch. reset
L	L	X	X	Asynch. preset
L	H	H	H	No change
L	H	↑	H	Count up
L	H	H	↑	Count down

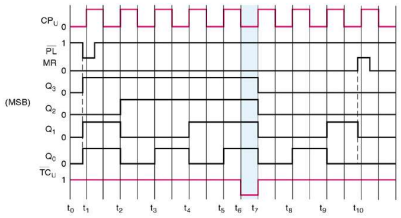
H = HIGH; L = LOW
X = Don't care; ↑ = PGT

(c)

Example



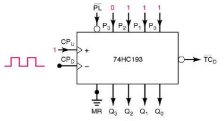
(a)



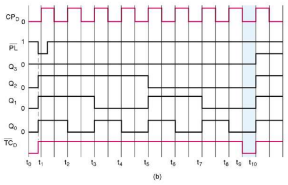
(b)

61

Example



(a)



(b)

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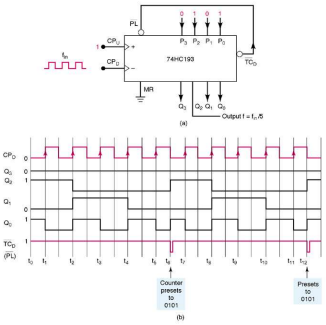
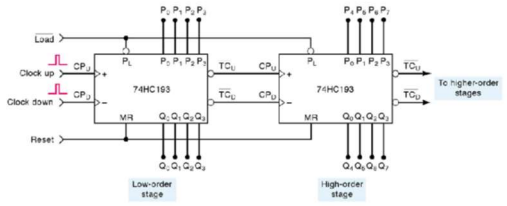
Variable MOD Number using the 74ALS193/HC193



(a) (b)

Multistage Arrangement



Note: Reset input has priority over Load and clock inputs.
Load input has priority over clock inputs.

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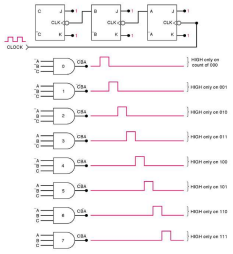
Review Questions

- Describe the function of the input PL and P_0 to P_3.
- Describe the function of the MR input
- True or False: The 74HC193 cannot be preset while MR is active.
- What logic levels must be present at CP_D, PL and MR in order for the 74ALS193 to count pulses that appear at CP_U?
- What would be the maximum counting range for a four-stage counter made up of 74HC193 Ics?

7-11 Decoding a counter

- Mentally decoding the binary states of the LEDs
  - Becomes inconvenient as the size of the counter increases
- Electronically decoding
  - To control the timing or sequencing of operations automatically without human intervention.
  - Active-High Decoding
  - Active-Low Decoding
  - BCD counter decoding

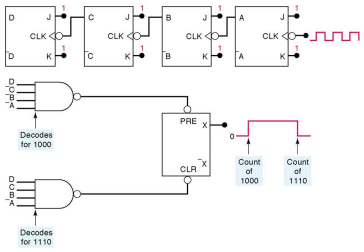
Active-High Decoding



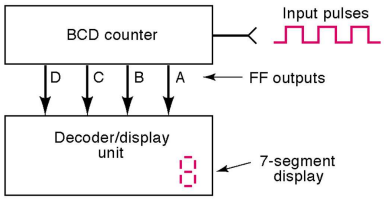
Example

- How many AND gates are required to decode completely all of the states of a MOD-32 binary counter? What are the inputs to the gate that decodes for the count of 21?

Active-LOW Decoding



BCD Counter Decoding



Review Questions

- **How many gates are needed to decode a six-bit counter fully?**
- **Describe the decoding gate needed to produce a LOW output when a MOD-64 counter is at the counter of 23.**

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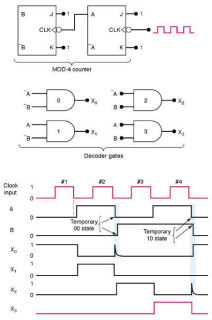
7-12 Decoding Glitches



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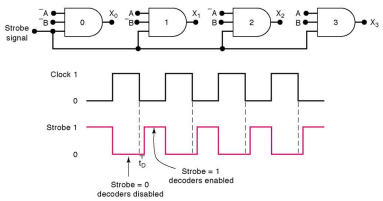
Strobing



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Review Questions

- **Explain why the decoding gates for an asynchronous counter may have glitches on their outputs.**
- **How does strobing eliminate decoding glitches?**

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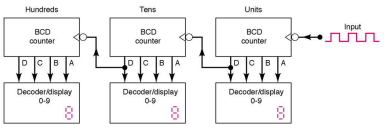
Cascading BCD counters



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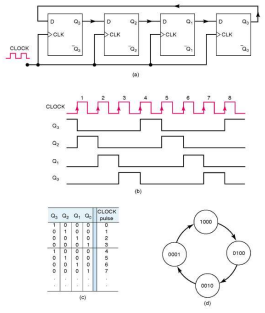
7-15 Shift-Register Counters



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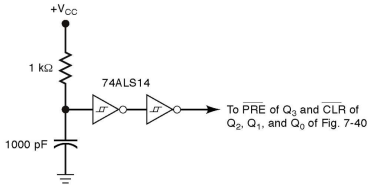
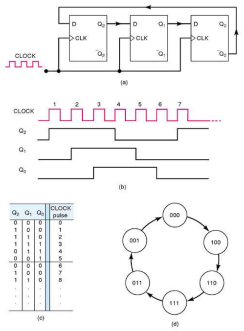
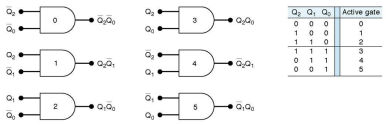
Starting a Ring Counter



Johnson Counter



Decoding A Johnson Counter



Q_2	Q_1	Q_0	Active gate
0	0	0	0
1	0	0	1
1	1	0	2
1	1	1	3
0	1	1	4
0	0	1	5

Review Questions

- Which shift-register counter requires the most FFs for a given MOD number?
- Which shift-register counter requires the most decoding circuitry?
- How can a ring counter be converted to a Johnson counter?
- True or False:
  - The outputs of a ring counter are always square waves.
  - The decoding circuitry for a Johnson counter is simpler than for a binary counter
  - Ring and Johnson counters are synchronous counters.
- How many FFs are needed in a MOD-16 ring counter? How many are needed in a MOD-16 Johnson Counter?