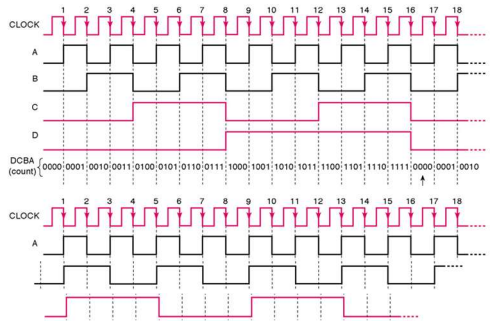
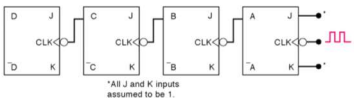
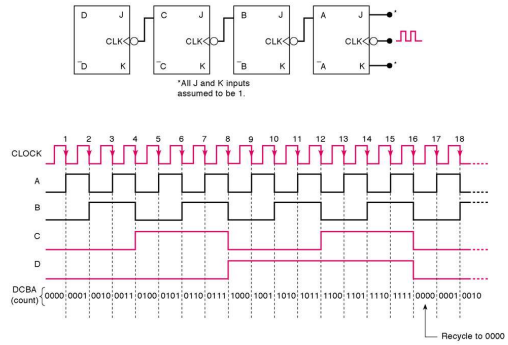
Chapter 7
Counters and Registers





7-1
Asynchronous (ripple) counters



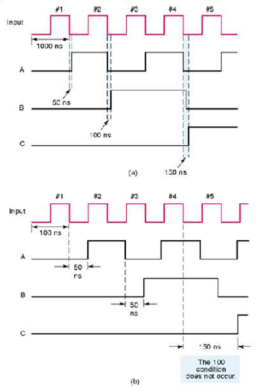
Asynchronous Counters (Cont.)

- Each FF output drives the CLK input of the next FF.
- FFs do not change states in exact synchronism with the applied clock pulses.
- *There is delay between the responses of successive FFS.*
- It is also often referred to as a *ripple counter* due to the way the FFs respond one after another in a kind of rippling effect.

Signal Flow

- It is conventional in circuit schematics to draw the circuits (whenever possible) such that the signal flow is from left to right, with inputs on the left and outputs one the right.
- In this chapter, we will often break with this convention, especially in diagrams showing counters.

7-5 Propagation delay in ripple counters



Discussion on Ripple Counter

- For proper counter operation, we need

$$T_{clock} \geq N \times t_{pd}$$

Asychronous counters are not useful at very high frequencies, especially for large number of bits.

Another problem caused by propagation delays in asychronous counters occurs when the counter outputs are decoded, as is discussed later.

Example

- The counter in Figure 7-1 starts off in the 0000 state, and then clock pulses are applied. Some time later the clock pulses are removed, and the counter FFs read 0011. *How many clock pulses have occurred*?

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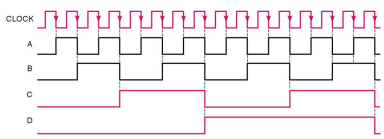
Answer:
3 or 19 or 163

N*16 + 3 (N is unknown)

MOD Number

- The counter in Figure 7-1 has 16 distinct states, thus, it is a MOD-16 ripple counter.
- The MOD number can be increased simply by adding more FFs to the counter. That is
  - MOD number = 2^N
- Example
  - A counter is needed that will count the number of items passing on a conveyor belt. A photocell and light source combination is used to generate a single pulse each time an item crosses its path. The counter must be able to count as many as one thousand items. How many FFs are required?

Frequency division



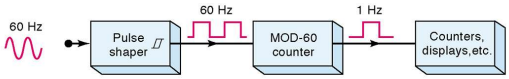
In any counter, the signal at the output of the last FF(i.e., the MSB) will have a frequency equal to the input clock frequency divided by the MOD number of the counter. Such circuits are known as *divide-by-N counters*.

13

Example

- The first step involved in building a digital clock is to take the 60-Hz signal and feed it into a Schmitt-trigger, pulse-shaping circuit to produce a square wave as illustrated in Figure 7-3. The 60HZ square wave is then put into a MOD-60 counter, which is used to divide the 60-HZ frequency by exactly 60 to produce a 1-HZ waveform. This 1-HZ waveform is fed to a series of counters, which then count seconds, minutes, hours, and so on. How many FFs are required for the MOD-60 counter?

14



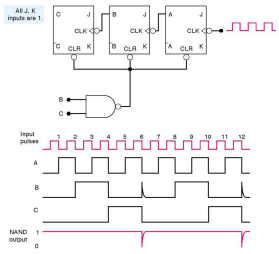
15

Review Questions

- True or False: In an asychronous counter, all FFs change states at the same time.
- Assume that the counter in Figure 7-1 is holding the count 0101. What will be the count after 27 clock pulses?
- What would be the MOD number of the counter if three more FFs were added?

16

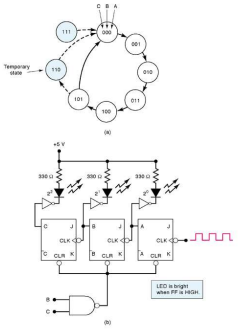
7-2 Counters with MOD NUMBER < 2^N



MOD-6 counter produced by clearing a MOD-8 counter when a count of six occurs.

17

State Transition Diagram



18

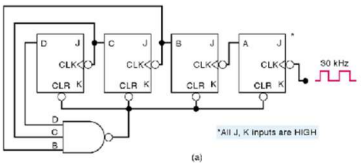
Example

- What will be the status of the LEDs when the counter is holding the count of five?
- What will the LEDs display as the counter is clocked by a 1-kHz input?
- Will the 110 state be visible on the LEDs?

19

Changing the MOD number

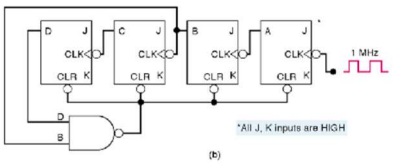
Determine the MOD number of the counter in Figure 7-6(a). Also determine the frequency at the D output



20

Changing the MOD number

Construct a MOD-__ counter that will count from 0000(zero) through 1001(decimal 9)



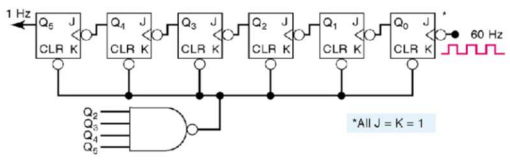
Decade Counters/BCD counters

- Decade counter
  - Any counter has 10 distinct states, no matter what the sequence.
- BCD counter
  - A decade counter counts in sequence from 0000(zero) through 1001(decimal 9).

22

Example

- Construct an appropriate MOD-__ counter.



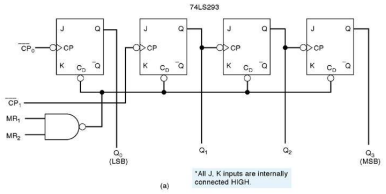
23

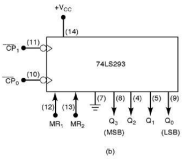
Review Questions

- What FF outputs should be connected to the clearing NAND gate to form a MOD-13 counter?
- True of False: All BCD counters are decade counters.
- What is the output frequency of a decade counter that is clocked from a 50-KHz signal?

24

7-3 IC Asynchronous counters



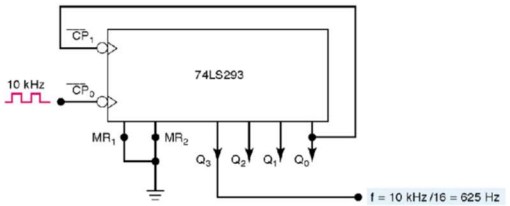


RESET IN		OUTPUT
$\overline{MR}_1$	$\overline{MR}_2$	$Q_3\,Q_2\,Q_1\,Q_0$
1	1	0 0 0 0
0	X	COUNT
X	0	COUNT

26

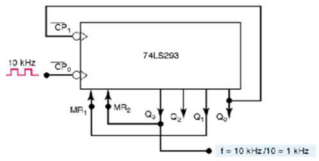
Example

- Show how the 74LS293 should be connected to operate as a MOD-16 counter with a 10-kHz clock input. Determine the frequency at Q_3.



Example

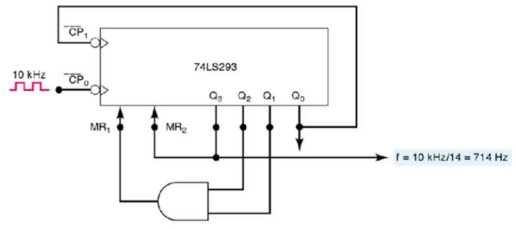
- Show how to wire the 74LS293 as a MOD-10 counter



28

Example

- Show how to wire a 74LS293 as a MOD-14 counter



29

Example

- A way to get a MOD-60 counter is shown below. Explain how this circuit works.

30

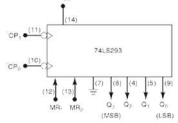
Review Questions

- Explain why a ripple counter's maximum frequency limitation decreases as more FFs are added to the counter.
- A certain J-K flip-flop has t_{pd}=12 ns. What is the largest MOD counter that can be constructed from these FFs and still operate up to 10 MHz?

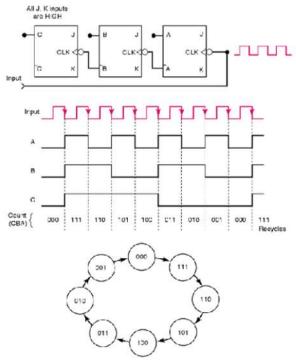
31

Review Questions

- A 2-kHz clock signal is applied to $\overline{CP_1}$ of a 74LS293. What is the frequency at Q_3?
- What would be the final output frequency if the order of the counters were reversed in Figure 7-12?
- What is the MOD number of a 74HC4040 counter?
- What would the notation "DIV64" mean on a counter symbol?
- Which outputs would you connect to an AND gate to convert the 74HC4024 to a MOD-120 counter?



7-4 Asychronous Down counter



33

Review Questions

- What is the difference between the counting sequence of an up counter and a down counter?
- Describe how an asynchronous down-counter circuit differs from an up-counter circuit.

34